

## REMARKS

The following is responsive to the Official Action mailed on October 28, 2005, and for which a two-month extension is hereby requested. The Office Action rejected claims 37 and 38 under 35 U.S.C. 102(b) as being anticipated by the "Flash Memory Products, 1992/1993 Data Book/Handbook, Advanced Micro Devices, Am29F010 ("AMD"), rejected claims 24- 27 and 34-36 under 35 U.S.C. 103(a) based on AMD in view of by Hazen et al. (U.S. patent number 5,280,447) or Lee et al. (U.S. patent number 5,796,657), and rejected claims 18-19, 22, 28-31, and 39-41 under 35 U.S.C. 103(a) based on AMD in view of Kaki et al. (U.S. patent number 5,809,515). For the reasons given below, it is respectfully submitted that these rejections are in error.

Claim 18 was objected to based on a repeated "system" in the preamble, which has now been deleted. Claim 33 was indicated as allowable if rewritten in independent form, which has now been done and claim 33 should therefore now be allowable.

### Claims 37 and 38

The Office Action rejected claims 37 and 38 under 35 U.S.C. 102(b) as being anticipated by the "Flash Memory Products, 1992/1993 Data Book/Handbook, Advanced Micro Devices, Am29F010 ("AMD"). It respectfully submitted that these rejections are in error on several bases.

Before going into the specific rejections, some general comments are given on the claims. The pending claims in the present application are drawn to two different sub-aspects of the present invention: claims 18, 39, and their dependent claims concern *erase*, while claims 24, 25, 37, and their dependent claims concern *write protection*. Both in the present Office Action and in earlier Office Actions, prior art elements related to one of these are cited against the other. These are quite different operations. For instance, in the present Office Action, for claims related to write protection, the Office Action will cite references or passages concerned entirely with *erase* that provide no teachings related to write protection. For instance, in the AMD reference, for limitations related *write protection claims*, the Office Action repeatedly refers to "Sector Erase section in 1-12" which, as is even clear from the way it is listed, is about *erase*.

Claim 37 states:

A memory system comprising:

a plurality of memory groups, each of said memory groups comprising a plurality of memory cells;

a plurality of *group tags*, each of said group tags corresponding to one of said memory groups, each of said group tags indicating whether the memory cells under the corresponding memory group are write protected; and

wherein any combination of the memory groups can be write protected and said *group tags are settable in response to a command from a host to which the memory system is connected.*

For the “group tags”, the Office Action cites page 1-3 of AMD, stating: “any combination of sectors can concurrently erased in 1-3 reads on this limitation”. *Claims 37 and 38 are not about erase*, but about write protection. Whether “any combination of sectors can be erased” is irrelevant to these claims. Also, there is no disclosure of the use of tags.

Concerning the limitation of “wherein ... said group tags are settable in response to a command from a host to which the memory system is connected”, the Office Action cites AMD “1-12 ‘Sector erase is a six bus cycle in sector erase’”. Again, *claims 37 and 38 are not about erase*, but about write protection. Page 1-12 of AMD completely concerns erase processes. Also, there is no disclosure of tags being set in response to a command from a host.

AMD does have some discussion of write protection, but this is found on page 1-10. However, as is clear from the “Sector Protection” section on that page, the ability to disable the program operation in sectors of the AMD device is *hardware* sector protection. It does not employ tags, but relies entirely on the hardware structure described in this section of AMD. Further, in AMD the ability to write protect is *not* “in response to a command from a host to which the memory system is connected”; rather, as is again clear for AMD’s “Sector Protection”, to write protect a sector must either be done as the manufacture or by using special programming equipment. This is no disclosure of a host being able to perform such a process.

For any of these reasons, it is respectfully submitted that a rejection of claim 37 under 35 U.S.C. 102(b) as being anticipated by the AMD reference is not well founded and should be withdrawn.

Concerning claim 38, as this depends on claim 37 it is believed allowable on this basis. It is further believed allowable as it contains the further limitation “wherein set ones of said group tags are deselected in response to command from said host.” The Office Action cites AMD page 1-10, which does refer to write protection; however, it has no disclosure of deselecting protected areas. In particular, it has no disclosure of deselecting “in response to command from said host.” As already discussed, this section of AMD only a *hardware* protection and

only to set the protection, a process not done by a host but which needs to be done at the factory or with special equipment.

#### Claims 24-27 and 34-36

##### Claim 24

The Office Action rejected claims 24- 27 and 34-36 under 35 U.S.C. 103(a) based on AMD in view of by Hazen et al. (U.S. patent number 5,280,447) or Lee et al. (U.S. patent number 5,796,657). Claim 24 reads:

A memory system comprising:  
a plurality of memory groups, each of said memory groups comprising a plurality of memory cells, wherein the number of memory cells in each memory group is configurable;  
a plurality of group tags, each of said group tags corresponding to one of said memory groups, each of said group tags indicating whether the memory cells under the corresponding memory group are write protected; and  
wherein any combination of the memory groups can be write protected.

For a “plurality of memory tags” and “write protected”, the Office Action again refers to AMD pages 1-3 and 1-12. As discussed above with respect to claim 37, this is incorrect and these cited locations are entirely concerned with erase processes. Further, as noted in the Office Action, “AMD does not specifically disclose the number of memory cells in each group is configurable.” (More accurately, AMD teaches away from any such configurability and the unit that can be write protected is the sector, a unit fixed in the hardware design of the device.) The Office Action uses the Lee and Hazen references to provide this limitation.

For the Hazen reference, the Office Action cites column 4, lines 39-42. But the cited portions of Hazen are again all concerned with *erase* structures, not *write* protection. Even the Office Action states that what Hazen discloses is “for the purpose of improving *erase* characteristics”, where the emphasis is added. Hazen does not disclose “the number of memory cells in each memory group is configurable” for write protection groups.

Similarly, for the Lee reference, the Office Action cites column 3, lines 30-40, and column 5, lines 13-16. But the cited portions of Lee are again all concerned with *erase* structures, not *write* protection. Even the Office Action states that what Lee discloses is “for the purpose of providing capability flexible *erasing* size”, where the emphasis is added. Lee does not disclose “the number of memory cells in each memory group is configurable” write protection groups.

For any of these reasons, it is respectfully submitted that a rejection of claim 24 under 35 U.S.C. 103(a) based on AMD and either of Lee or Hazan is not well founded and should be withdrawn.

#### Claim 25

As for claim 25, this contains all the limitations of claim 24, except for “wherein the number of memory cells in each memory group is configurable”, replacing it with “wherein the corresponding cells in each memory group are calculated in real time”. Claim 24 reads:

A memory system comprising:  
a plurality of memory groups, each of said memory groups comprising a plurality of memory cells, wherein the corresponding cells in each memory group are calculated in real time;  
a plurality of group tags, each of said group tags corresponding to one of said memory groups, each of said group tags indicating whether the memory cells under the corresponding memory group are write protected; and  
wherein any combination of the memory groups can be write protected.

For a “plurality of memory tags” and “write protected”, the Office Action again refers to AMD pages 1-3 and 1-12. As discussed above with respect to claim 37, this is incorrect and these cited locations are entirely concerned with erase processes. Further, as noted in the Office Action, “AMD does not specifically disclose the corresponding cells in each memory group is calculated in real time.” (More accurately, AMD teaches away from any such configurability and the unit that can be write protected is the sector, a unit fixed in the hardware design of the device.) The Office Action also uses the Lee and Hazan references to provide this limitation.

For the Hazan reference, the Office Action cites column 4, lines 25-42. As before, the cited portions of Hazan are again all concerned with *erase* structures, not *write* protection. Even the Office Action states that what Hazan discloses is “for the purpose of improving *erase* characteristics”, where the emphasis is added. Further, what Hazan describes in the cited location is a “configuration cell” that can either be in a first voltage state or second voltage state that determines if a block is to be erased. Thus, this is more a case of “setting group tags” (although here for an erase process instead of write protect), rather than calculating the “corresponding cells in each memory group in real time”.

Similarly, for the Lee reference, the Office Action cites column 5, lines 30-50, and column 5, lines 13-16. But the cited portions of Lee are again all concerned with *erase* structures, not *write* protection. Even the Office Action states that what Lee discloses is “for the

purpose of providing capability flexible *erasing* size”, where the emphasis is added. In the cited location Lee describes the use latches that determine whether erase occurs or is inhibited. Lee does not disclose calculating the “corresponding cells in each memory group in real time” for write protect group.

For any of these reasons, it is respectfully submitted that a rejection of claim 25 under 35 U.S.C. 103(a) based on AMD and either of Lee or Hazan is not well founded and should be withdrawn.

#### Claims 26, 27 and 34-36

All of claims 26, 27, and 34-36 are dependent claims having either claim 24 or 25 as their base claim and consequently believed allowable on this basis alone. Many of these claims recite further limitations for which it is believed they are further allowable.

For example, claims 34-36 respectively have the limitations of “wherein said group tags are settable by a host to which the memory system is connected”, “wherein said group tags are set in response to a host command”, and “wherein set ones of said group tags are deselected in response to a host command.” These are similar to limitations found in claims 37 and 38 that were discussed above and have been rejected on the same basis by the Office Action; as before, it is believed that these rejections are in error and that claims 34-36 are further allowable for the reasons given above with respect to claims 37 and 38.

#### Claims 18-19, 22, 28-31, and 39-41

The Office Action rejected claims 18-19, 22, 28-31, and 39-41 under 35 U.S.C. 103(a) based on AMD in view of Kaki et al. It respectfully submitted that these rejections are in error and should be withdrawn. These claims are all drawn to the erase structure found in the device of the present application, a structure that is neither found in nor obvious from the AMD or Kaki references, either alone or taken together.

The structure found in these claims describes a memory that has a plurality of groups; each group has a plurality of sectors/units of erase; and each sector/unit of erase is composed of multiple cells. Thus, there are *two* levels of structure between the cell and the memory, the group and the sector/unit of erase, with a tag for each of the elements at *both* of these levels.

Any combination of groups, and any combination of sectors/units of erase in any group, can have their erase tag set and then all erased simultaneously.

Concerning the AMD reference, beginning on page 1-3, this describes a first device (Am29F010) that is composed on multiple sectors. As described on page 1-3 and, in more detail, on pages 1-11 and 1-12, this device can be erased at the chip level and at the sector level for multiple sectors. However, it only has this single intermediate level of the sector between the cell level and the entire chip. There is neither disclosure nor suggestion of another intermediate layer corresponding to the “group” of the claims. Beginning on page 3-38, AMD presents a *different* device (AmC002FLKA). As described on page 3-48, this device only erases at the level of the entire array and on 256K byte segments. There is also neither disclosure nor suggestion of another intermediate layer corresponding to the “group” of the claims for this device. In its comments, the Office Action refers to the “memory groups” of the claims corresponding to S0-S7 on page 3-39, further stating that each of these S0-S7 have a plurality of sectors as disclosed on page 1-4. It is again noted that the device on page 3-39 *is a different device* from that found on page 1-4. Further, there is no disclosure in AMD the S0-S7 have any sort of association with what is defined by the claims as a “group”.

As for the Kaki reference, this also only describes the structure of a chip having multiple sectors (the unit of erase), where each sector has multiple cells. Kaki neither discloses nor suggests the introduction of another intermediate layer corresponding to the “group” of the claims. Beginning at line 64 of column 7, Kaki considers where there unit of erase may be a different size than a sector (this is done for consideration of how it affects the “write management table”), but still only considers a single intermediate level (the erase unit) between the entire array and the cell. There is again no discussion of the concurrent use of a second, distinct intermediate level corresponding to the “group” of the claims.

Further, as for “any combination of the memory groups can be simultaneously erased”, this is not only *not* taught by Kaki, but is *directly contrary* to what Kaki teaches. In its comments, the Office Action refers column 7, lines 28-30, which state “the plurality of flash memories 4 are erased in parallel”; however, these are different memory arrays that are erased in parallel. As described with respect to Figure 4 beginning at line 32 of column 7, for each of these parallel erase operations only a single sector/unit of erase is being erased at a time; that is, within a given flash memory 4, the sectors are erased *sequentially* and only one sector at time

can be erased. In Figure 4 of Kaki, this is function of the loop from diamond 45 back up to above boxes 43 and 44. In Kaki, the in “parallel” is for different arrays, but in each array the units of erase are only done sequentially as is clear from text.

#### Claim 18

Concerning claim 18 specifically, this contains both the sector and “group” level structures described in the preceding paragraphs. The Office Action cites AMD at 3-39 and 1-4 for the “group” and sector structures, respectively. As described in the preceding discussion, the cited locations in AMD refer to two different devices, neither of which either teaches or suggests the use of the sort of “group” found in the claims.

The Office Action correctly notes that AMD does not disclose that any combination of memory groups can be simultaneously erased, for which it turns to the Kaki reference. However, as described in the preceding discussion, Kaki lacks a “group” structure and instead only has the sector (unit of erase) and explicitly teaches that such sectors must be erase *sequentially*.

Consequently, for any of these reasons, it is respectfully submitted that a rejection of claim 18 under 35 U.S.C. 103(a) based on AMD and Kaki is not well founded and should be withdrawn.

#### Claims 19, 22, and 28-31

All of claims 19, 22, and 28-31 are dependent claims having claim 18 as their base claim and consequently believed allowable on this basis alone. Many of these claims recite further limitations for which it is believed they are further allowable.

Concerning claim 19, this has the additional limitation of “wherein the corresponding sectors in each memory group is calculated in real time”, for which the Office Action cites AMD at 1-25. However, this section of AMD is about *protection* of sectors from erase, not arranging of sectors in “group” structure so that they *can* be erased. Also, this is a *hardware* arrangement that either must be done at the factor or using special equipment (see AMD page 1-10); consequently, it is not something that can be performed “in real time”. Further, as already discussed, AMD lacks any corresponding “group” structure and all arrangements of erase structures are fixed in hardware according to the design, so that there is no such corresponding concept to even be computed, whether in real time or otherwise.

As for claims 28 and 29, it is again noted that these specify both sector tags and group tags, where both the group structure and, thus, any corresponding tags are not found in AMD or Kaki.

As for claim 30, this has the additional limitation of “wherein set ones of said sector tags and said group tags are deselected in response to a host command”, for which the Office Action cites AMD at 1-25. However, this section of AMD is about *protection* of sectors from erase, *not* the selecting and deselecting of sectors or “groups” so that they *can* be erased. Also, this is a *hardware* arrangement that either must be done at the factor or using special equipment (see AMD page 1-10); consequently, it is not something done “in response to a host command”.

Concerning claim 31, this has the additional limitation of “wherein the number of memory sectors in each memory group is configurable by a host to which the memory system is connected”, for which the Office Action cites AMD at 1-25. However, this section of AMD is about *protection* of sectors from erase, not arranging of sectors into a “group” structure so that they *can* be erased. Also, this is a *hardware* arrangement that either must be done at the factor or using special equipment (see AMD page 1-10); consequently, it is not something that can be performed by a host. Further, as already discussed, AMD lacks any corresponding “group” structure and all arrangements of erase structures are fixed in hardware according to the design, so that they cannot be configured as described in the claim.

#### Claims 39-41

Claims 39 and 40 are method claims that respectively correspond claim 18 and 31, are rejected by the Office Action on the same basis, and are, consequently, believed allowable for the same reasons as these claims.


As for claim 41, this has the limitation of “wherein the size of the groups is stored in a register on card.” The Office Action just makes a general statement that AMD discloses this feature, but does not provide any indication of where in AMD it can be found. As far as can be determined, AMD is entirely lacking in any disclosure or teaching of such a limitation. Further, as AMD has no structure corresponding to the “group” of the claim and as all erase structures in AMD are fixed in hardware and not configurable, not only is the limitation of the claim not found in AMD, but it is unclear what purpose it could serve.



Conclusion

Therefore, for any of the above reasons, it is respectfully submitted that a rejection of claims 18, 19, 22, 24-31, and 34-41 under the stated reasons is not well founded and should be withdrawn. Reconsideration of claims 18, 19, 22, 24-31, and 34-41 and an early indication of their allowance are respectfully requested.

Respectfully submitted,

  
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